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EXAMINER	
KUNZER, BRIAN	
ART UNIT	**PAPER NUMBER**
2814	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/808,389	KONISHI ET AL.	
	Examiner	Art Unit	
	Brian Kunzer	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) *9-13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Amendments

The remarks and amendments filed on January 17th, 2006 have been received and entered. In summary, claims 1, 2, and 8 have been amended and claims 9-13 have been cancelled.

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "Stacked RF Module with Multi-Frequency Opposed Circuits"

Claim Objections

Claim 8 is objected to because of the following informalities: Claim 8 recites the limitation, "extending in a direction intersecting a direction in which the first ***pads*** of the second semiconductor chip are arranged." However there is no previous mention of limitation "pads". Examiner believes this to be a typing error and "pads" should be replaced with "electrodes". Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1, 4, 5, 7, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tarui (US Patent No. 6,657,523) in view of Winslow (US Patent No. 6,803,817).

With respect to claim 1, Tarui teaches, from fig. 1, a semiconductor device comprising:

a printed wiring board (1a) having a top surface, and a backside surface, on the side of the printed wiring board, opposite from the top surface;

a second semiconductor chip (9c and 9d) mounted over the top surface of the printed wiring board (1a) including first circuits (9c) operated at a first frequency and second circuits (9d) operated at a second frequency;

wherein the first frequency is distinct from the second frequency; (separate modulations – in amplitude, phase or frequency - occur in each MMIC chip 9a-9d, see column 8, lines 1-22)

a first semiconductor chip (9a and 9b) disposed so as to overlie the second semiconductor chip (9c and 9d) including a first circuit (9a) and a second circuit (9b);

wherein the first circuit is independent of the second circuit of the first semiconductor chip; (separate modulations – in amplitude, phase or frequency - occur in each MMIC chip 9a-9d, see column 8, lines 1-22)

a plurality of conductive wires (13 also with conductive vias 5c and 5d) electrically bonding the first semiconductor chip (9a and 9b) to the printed wiring board (1a);

wherein the first circuit (9a) of the first semiconductor chip is disposed opposite to the second circuits (9d) of the second semiconductor chip, while the second circuit (9b) of the first

semiconductor chip is disposed opposite to the first circuits (9c) of the second semiconductor chip.

However, Tarui does not explicitly teach that the first and second circuits can be formed in the same chip (i.e. Tarui shows the two circuits (9a and 9b) in the first chip and the two circuits (9c and 9d) in the second chip as four separate chips).

Winslow, drawn to dual band power amplifiers, teaches, from fig. 2, a semiconductor device with a single chip including first circuits (14b) operated at a first frequency and second circuits (14a) operated at a second frequency. (see column 3, lines 48-51)

Therefore it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the stacked arrangement of Tarui with the device of Winslow - a stack creating a dual band amplifier - because the arrangement would reduce the area covered by the power amplifier circuit on the printed wiring board, thus consuming less space, making further miniaturization of devices (such as cell phones) possible both by stacking the chips and by placing two different band amplifiers in the same chip. (See column 1, lines 15-18 in 6,803,817 and also column 3, lines 9-48 in 6,657,523.)

With respect to claim 4, Winslow teaches the first and second frequencies are in the ranges of 880 ~ 915 MHz and 1710 ~1785 MHz., respectively. (see column 1, lines 27-31)

With respect to claim 5, Tarui teaches, from fig. 1, the said semiconductor device wherein the second semiconductor chip (9c and 9d) is electrically bonded to the printed wiring board (1a) with conductive wires (13).

With respect to claim 7, Tarui combined with Winslow teach, from figs. 1-3, the said semiconductor device, wherein a first wire (13a) that is electrically bonded to the first circuit (9a) of the first semiconductor chip (9a and 9b) is disposed opposite to a first wiring (13f) of the printed wiring board (1a), which is electrically bonded to the second circuits (9d) of the second semiconductor chip (9c and 9d), respectively, while a second wire (13c) that is electrically bonded to the second circuit (9b) of the first semiconductor chip (9a and 9b) is disposed opposite to a second wiring (13d) of the printed wiring board (1a), which is electrically bonded to the first circuits (9c) of the second semiconductor chip (9c and 9d), respectively.

With respect to claim 8, Tarui teaches, from figs. 1-3, a semiconductor device comprising:

a printed wiring board (1a) having a top surface, and a backside surface, on the side of the printed wiring board, opposite from the top surface;

a second semiconductor chip (9c and 9d) mounted over the top surface of the printed wiring board (1a) including first circuits (9c) operated at a first frequency and second circuits (9d) operated at a second frequency, a plurality of first electrodes (2j, 2k, 4h) bonded to the first circuits (9c), respectively, and a plurality of second electrodes (2l, 2m, 4i) bonded to the second circuits (9d), respectively,

wherein the first frequency is distinct from the second frequency; (separate modulations – in amplitude, phase or frequency - occur in each MMIC chip 9a-9d, see column 8, lines 1-22)

a first semiconductor chip (9a and 9b) disposed so as to overlie the second semiconductor chip (9c and 9d) including a first circuit (9a) and a second circuit (9b), a plurality of first electrodes (2d, 2e, 4m) bonded to the first circuits (9a), respectively, and a plurality of second electrodes (2f, 2g, 4l) bonded to the second circuits (9b), respectively,

wherein the first circuit is independent of the second circuit of the first semiconductor chip; (separate modulations – in amplitude, phase or frequency - occur in each MMIC chip 9a-9d, see column 8, lines 1-22) and

a plurality of wires (13) electrically bonding the first semiconductor chip (9a and 9b) and the second semiconductor chip (9c and 9d) to the printed wiring board (1a), respectively;

wherein the plurality of wires (13) bonded to the plurality of first electrodes and second electrodes of the first semiconductor chip, respectively, are disposed so as to cross a pair of edges, that are opposed to each other, of a top surface of the first semiconductor chip (far left and far right edges of 9a and 9b respectively), extending in a direction intersecting a direction in which the first electrodes of the second semiconductor chip are arranged, and

wherein the plurality of wires (13) bonded to the plurality of first electrodes and second electrodes of the second semiconductor chip, respectively, are disposed so as to cross a pair of edges, that are opposed to each other, of a top surface of the second semiconductor chip (far left and far right edges of 9c and 9d respectively), extending in a direction intersecting a direction in which the first electrodes of the first semiconductor chip are arranged.

However, Tarui does not explicitly teach that the first and second circuits can be formed in the same chip (i.e. Tarui shows the two circuits (9a and 9b) in the first chip and the two circuits (9c and 9d) in the second chip as four separate chips).

Winslow, drawn to dual band power amplifiers, teaches, from fig. 2, a semiconductor device with a single chip including first circuits (14b) operated at a first frequency and second circuits (14a) operated at a second frequency. (see column 3, lines 48-51)

Therefore it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the stacked arrangement of Tarui with the device of Winslow - a stack creating a dual band amplifier - because the arrangement would reduce the area covered by the power amplifier circuit on the printed wiring board, thus consuming less space, making further miniaturization of devices (such as cell phones) possible both by stacking the chips and by placing two different band amplifiers in the same chip. (See column 1, lines 15-18 in 6,803,817 and also column 3, lines 9-48 in 6,657,523.)

2. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tarui (US Patent No. 6,657,523) in view of Winslow (US Patent No. 6,803,817) as applied to claim 1 above, and further in view of Jaakola (US Patent No. 5,884,149).

Tarui in combination with Winslow teach the semiconductor device of claim 1.

However, Tarui in combination with Winslow do not specifically teach the semiconductor device operating at more than two frequencies in a single chip.

Jaakola, drawn to multi-band amplifiers, teaches, from column 7, lines 8-20, that a dual band amplifier circuit could easily be transformed into a quad-band circuit (enabling four separate frequency bands to be received/transmitted) by incorporating additional known circuitry.

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to use the combined device arrangement suggested by Tarui and Winslow in conjunction with the circuits of Jaakola, because this simply allows amplification of more frequency bands, thus providing reception for more telecommunication systems. (See column 7, lines 8-20.)

3. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tarui (US Patent No. 6,657,523) in view of Winslow (US Patent No. 6,803,817) as applied to claim 1 above, and further in view of Arai (US Patent No. 6,753,735).

Tarui in combination with Winslow teach the semiconductor device of claim 1.

However, Tarui in combination with Winslow do not specifically teach the semiconductor device further comprising amplifier circuits for amplifying input signals in three stages, wherein the amplifier circuits in the initial stage of the three stages are installed in the first semiconductor chip, and the amplifier circuits in second and third stages, respectively, are installed in the second semiconductor chip. Although Tarui does teach that the MMICs 9a-9d are capable of amplifying signals and therefore three different MMIC's could logically be three amplifiers that amplify input signals in three stages.

Nevertheless, Arai, drawn to power amplifier modules, teaches, from figs. 9 and 10, three stage amplifiers that are employed in different chips including the first and second stage amplifiers (210b or 210a) and the third stage amplifiers (213a,b) being in separate chips.

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to use the combined device arrangement suggested by Tarui and Winslow in

conjunction with the three stage amplifier stacked in different chips in order to provide separate power requirements to the amplifiers. (See column 10, lines 29-39.)

4. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tarui (US Patent No. 6,657,523) in view of Winslow (US Patent No. 6,803,817) as applied to claim 1 above, and further in view of Rostoker (US Patent No. 5,457,878).

Tarui in combination with Winslow teach the semiconductor device of claim 1.

Tarui in combination with Winslow do not specifically teach the semiconductor device wherein the second semiconductor chip is bonded to the printed wiring board by flip bonding.

However, Rostoker, drawn to mounting IC chips onto circuit boards, teaches from fig. 1 and column 6, lines 44-48, a number of different ways to attach an IC chip to a board including flip chip bonding.

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the combined device of Tarui and Winslow wherein the second chip was flip chip bonded - as opposed to wire bonded - to the board, as taught by Rostoker, since this is just a different, yet functional equivalent, way of bonding a chip to a board and its application is well known in the art. (See column 6, lines 44-48.)

Response to Arguments

5. Applicant's arguments with respect to claims 1-8 have been considered but are moot in view of the new ground(s) of rejection. The new grounds of rejection are due to the amendment

of independent claims 1 and 8 wherein Lo nor Kamikuri teach more than one independent circuit in the first semiconductor chip.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Kunzer whose telephone number is (571) 272-5054. The examiner can normally be reached on Monday-Friday 8:00-4:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BK
3/23/2006

ANH D. MAI
PRIMARY EXAMINER